formed to a depth sufficient to remove the charge-carrier dopant impurities implanted to form source/drain region **214**, as depicted in FIG. **2**E.

[0026] Referring to FIG. **2**F, epitaxial source/drain region **218** may be formed selectively in etched-out region **216** from FIG. **2**E. In accordance with an embodiment of the present invention, epitaxial source/drain region **218** is a strain-inducing semiconductor region that imparts a compressive uniaxial strain to substrate **204** and, hence, to channel region **212**. In another embodiment, epitaxial source/drain region **218** is a strain-inducing semiconductor region that imparts a tensile uniaxial strain to substrate **204** and, hence, to channel region **212**. In one embodiment, substrate **204** is comprised of Si_xGe_{1-x} where $0 \leqq x \leqq 1$ and epitaxial source/drain region **218** is comprised of Si_yGe_{1-y} where $0 \leqq y \leqq 1$ and $y \neq x$. In another embodiment, substrate **204** is comprised of silicon and epitaxial source/drain region **218** is comprised of carbon-doped silicon. In an embodiment, the top surface of epitaxial source/drain region **218** is raised above the top surface of crystalline substrate **204**, as depicted in FIG. **2**F.

[0027] In accordance with an embodiment of the present invention, charge-carrier dopant impurity atoms are implanted into epitaxial source/drain region **218** either during (i.e. in situ) or subsequent to the formation of epitaxial source/drain region **218**. In one embodiment, epitaxial source/drain region **218** is comprised of Si_xGe_{1-x} where $0 \leqq x \leqq 1$ or carbon-doped silicon and the charge-carrier dopant impurity atoms implanted are selected from the group consisting of boron, arsenic, indium or phosphorus. In another embodiment, epitaxial source/drain region **218** is comprised of a III-V material and the charge-carrier dopant impurity atoms implanted are selected from the group consisting of carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

[0028] Referring to FIG. **2**G, sacrificial isolation spacers **235** may be removed by any suitable technique that does not significantly impact substrate **204**, including tip extensions **210** and epitaxial source/drain regions **218**, gate dielectric layer **208** or gate electrode **202**. In accordance with an embodiment of the present invention, sacrificial isolation spacers **235** are removed by a dry etch or wet etch process. In one embodiment, sacrificial isolation spacers **235** are comprised of silicon dioxide, silicon oxy-nitride, carbon-doped silicon oxide or a low-temperature furnace oxide and are removed with a wet etch comprising aqueous hydrofluoric acid, ammonium fluoride or both. In another embodiment, sacrificial isolation spacers **235** are comprised of silicon nitride or carbon-doped silicon nitride and are removed with a wet etch comprising aqueous phosphoric acid. In accordance with an embodiment of the present invention, upon removal of sacrificial isolation spacer **235**, a trench **240** is formed directly between epitaxial source/drain region **218** and gate electrode **202**, as depicted in FIG. **2**G. In one embodiment, trench **240** has a height in the range of 50-1000 Angstroms.

[0029] The structure from FIG. **2**G provides a framework for a replacement isolation spacer. In accordance with an embodiment of the present invention, referring to FIG. **2**H, a material layer **250** is deposited by a chemical vapor deposition process and is conformal with the structure formed in FIG. **2**G. Material layer **250** will ultimately be used to form the lower portion of a multi-component isolation spacer and is therefore comprised of a material that could be detrimentally impacted during typical processing steps (such as ion bombardment implant steps, wet chemical cleans steps and dry etch steps). In one embodiment, material layer **250** is comprised of an insulating layer. In a particular embodiment, material layer **250** is comprised of silicon dioxide, a porous film or a fluorinated oxide. In another embodiment, material layer has a dielectric constant in the range of 2.0-4.0. In one embodiment, material layer has a dielectric constant in the range of 2.5-3.5. Material layer **250** may be deposited to a thickness sufficient to fill trench **240**. In an embodiment, material layer **250** is deposited to a thickness in the range of 30-250 Angstroms.

[0030] Referring to FIG. **2**I, all portions of material layer **250** that are not in trench **240** may be removed to provide lower portions **255** of a replacement low-k isolation spacer. In accordance with an embodiment of the present invention, lower portions **255** are flush with the top surface of epitaxial source/drain regions **218**, as depicted in FIG. **2**I. In one embodiment, a wet etch process step comprising the application of an aqueous solution of hydrofluoric acid, ammonium fluoride or both may be used to remove those portions of material layer **250** that are not in trench **240**.

[0031] Upper portions of a replacement low-k isolation spacer may then be formed by any suitable technique that provides a dielectric layer directly adjacent to the sidewalls of gate electrode **202** and above lower portions **255**. In accordance with an embodiment of the present invention, referring to FIG. **2**J, a material layer **260** is deposited by a chemical vapor deposition process and is conformal with the structure formed in FIG. **2**I. In one embodiment, material layer **260** is comprised of an insulating layer. In a particular embodiment, material layer **260** is comprised of silicon dioxide, silicon oxy-nitride, carbon-doped silicon oxide, silicon nitride, carbon-doped silicon nitride or a combination thereof. In another embodiment, material layer **260** has a dielectric constant in the range of 4.0-7.5. In an embodiment, material layer **260** has a dielectric constant at least twice the dielectric constant of lower portion **255**. Material layer **260** may be deposited to a thickness selected to determine the final width of the upper portion of a replacement low-k isolation spacer. In one embodiment, material layer **260** is deposited to a thickness in the range of 40-400 Angstroms.

[0032] Referring to FIG. **2**K, upper portions **265** of a replacement low-k isolation spacer **270** are formed from material layer **260** by, for example, an anisotropic etch process. In one embodiment, material layer **260** is dry etched by a remote plasma etch or a reactive ion etch process. In another embodiment, material layer **260** is patterned to form upper portions **265** by using a vertical dry or plasma etch process comprising fluorocarbons of the general formula C_xF_y, where x and y are natural numbers. In another embodiment, material layer **260** is patterned to form upper portions **265** by using a vertical dry or plasma etch process comprising free radical fluorocarbons. In accordance with an embodiment of the present invention, upper portions **265** have a slower etch rate than, i.e. are more robust than and hence protect, lower portions **255**. Upper portion **265** sit directly above the top surface of lower portion **255** of replacement low-k isolation spacer **270** and may have a width at the top surface of lower portion **255** substantially equal to the original thickness of material layer **260**. In accordance with an embodiment of the present invention, upper portions **265** of replacement low-k isolation spacer are